

Application No. 10/675,740
Response to OA of 04/20/2005

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (currently amended) A resistive cross point memory, comprising:
an array of memory cells; and
a read circuit comprising a charge amplifier and configured to sense a resistance through a memory cell in the array of memory cells to obtain a sense result and adjust the read circuit based on the sensed result, where the read circuit comprises an up/down counter that provides a calibration value to the charge amplifier-read circuit.
2. (original) The resistive cross point memory of claim 1, where the up/down counter is configured to provide a coarse calibration value in a complete calibration of the read circuit.
3. (original) The resistive cross point memory of claim 1, where the up/down counter is configured to provide a fine calibration value in a complete calibration and in a tune-up calibration of the read circuit.
4. (original) The resistive cross point memory of claim 1, where the read circuit is configured to provide a complete calibration that provides adjustments to a coarse calibration value and a fine calibration value.
5. (original) The resistive cross point memory of claim 1, where the read circuit is configured to provide a tune-up calibration that provides an adjustment to a fine calibration value.
6. (original) The resistive cross point memory of claim 1, where the up/down counter receives a single clock pulse to adjust a fine calibration value in a tune-up calibration.
7. (currently amended) A resistive cross point memory, comprising:

Application No. 10/675,740
Response to OA of 04/20/2005

an array of memory cells; and
a read circuit configured to sense a resistance through a memory cell in the array of
memory cells to obtain a sense result and adjust the read circuit based on the sensed
result, where the read circuit comprises an up/down counter that provides a calibration
value to the read circuit. ~~The resistive cross point memory of claim 1, where the up/down~~
counter is preset to an initial calibration value.

8. (original) The resistive cross point memory of claim 1, where the up/down counter is an up/down ripple counter.

9. (canceled)

10. (original) The resistive cross point memory of claim 1, where the read circuit comprises an integrator for obtaining a sense result.

11. (currently amended) The resistive cross point memory of claim 1, where the read circuit comprises:

a sense amplifier;
~~a charge amplifier;~~
a capacitor electrically coupled to the sense amplifier and the charge amplifier;
and
a switch electrically coupled to the sense amplifier, the charge amplifier, and the capacitor.

12. (original) The resistive cross point memory of claim 1, where the resistive cross point memory is a magnetic random access memory.

13. (original) A magnetic memory comprising:

a memory cell;
a charge amplifier configured to provide a sense voltage to the memory cell and integrate a sense current through the memory cell;

Application No. 10/675,740
Response to OA of 04/20/2005

a sense amplifier configured to sense integration time and provide a sense result;
and

an up/down counter configured to provide a calibration value to the charge
amplifier.

14. (original) The magnetic memory of claim 13, where the up/down counter is
configured to provide the calibration value to adjust back gate bias voltages on transistor
wells in the charge amplifier.

15. (original) The magnetic memory of claim 13, where the up/down counter is
configured to provide the calibration value to adjust impedances in the charge amplifier.

16. (original) The magnetic memory of claim 13, where the sense amplifier comprises a
counter that provides the sense result as a sense count.

17. (original) The magnetic memory of claim 13, where the sense amplifier comprises
threshold values that are compared to the sense result to determine charge amplifier
calibration needs, where the up/down counter receives a clock signal to change the
calibration value in the event the sense result exceeds one of the threshold values.

18. (original) The magnetic memory of claim 13, where the charge amplifier comprises:
a plurality of transistors that provide a controlled current path, with at least two of
the transistors situated in isolated wells; and

a calibration circuit responsive to a value in the up/down counter to provide at
least one of the following: a back gate bias voltage to at least one isolated well and
adjusting the impedance of the transistors providing the controlled current path, where
the level of the back gate bias voltage and the amount of impedance adjustment is
determined by the value of the up/down counter.

19. (currently amended) A magnetic memory, comprising:
means for sensing a resistance through a memory cell;

Application No. 10/675,740
Response to OA of 04/20/2005

means for comparing the sensed resistance to a threshold value; and
means for modifying a count in an up/down counter that provides a calibration
value to calibrate a read circuit to improve reliability of read operations
means for coarse calibration of the read circuit; and
means for fine calibration of the read circuit.

20. (canceled)

21. (original) The magnetic memory of claim 19, further comprising:
means for performing an initial calibration of the read circuit;

means for providing a complete calibration of the read circuit;

and

means for providing a tune-up calibration of the read circuit.

22. (original) A method of calibrating a magnetic memory, comprising:
sensing a resistance through a memory cell to obtain a sense result;
comparing the sense result to threshold values; and
clocking an up/down counter to adjust a calibration value.

23. (original) The method of claim 22, where comparing the sense result comprises
comparing the sense result to threshold values that are predetermined threshold values
around each resistive state of the memory cell.

24. (original) The method of claim 22, where comparing the sense result comprises
comparing a first sense result to threshold values, where the threshold values determine
complete calibration regions, tune-up calibration regions and a no calibration region.

25. (original) The method of claim 22, where sensing a resistance comprises obtaining a
sense count that represents an integration time for a voltage on a capacitor to reach a
reference voltage.

Application No. 10/675,740
Response to OA of 04/20/2005

26. (original) The method of claim 22, where sensing a resistance comprises:

- applying a voltage across a selected bit line and a selected word line crossing a selected memory cell; and
- applying an array voltage to unselected word lines and bit lines to reduce parasitic currents.

27. (original) A method for calibrating a read circuit in a resistive cross point memory comprising:

- providing an up/down counter;
- selecting a resistive cross point memory cell;
- sensing resistance through the selected resistive cross point memory cell in a sense operation;
- obtaining a sense result that represents an integration time for the sense operation;
- comparing the sense result to a threshold value; and
- applying a clock signal to the up/down counter in the event the sense result exceeds the threshold value.

28. (original) The method of claim 27, where the resistive cross point memory cell is a magnetic random access memory cell.

29. (previously presented) A method comprising:

- calibrating a read circuit in a magnetic memory to improve read operations of the read circuit by:
- performing a first sense operation and obtaining a first sense result;
- comparing the first sense result to first and second upper threshold values and to first and second lower threshold values, where the first upper threshold value is greater than the second upper threshold value and the first lower threshold value is less than the second lower threshold value;

Application No. 10/675,740
Response to OA of 04/20/2005

providing a clock pulse to an up/down counter if the first sense result is one of the following: greater than the second upper threshold value and less than the second lower threshold value;

performing a second sense operation and obtaining a second sense result if the first sense result is one of the following: greater than the first upper threshold value and less than the first lower threshold value; and

comparing the second sense result to the first and second upper threshold values and to the first and second lower threshold values.

30. (original) The method of claim 29, where the magnetic memory is a magnetic random access memory.